REMARKS

In the December 19, 2006 Office Action, claims 47-48 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 1, 47 and 48 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,826,971 to Hirose ("Hirose '971"). Claims 36, 37, 40, 43 and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hirose '971 in view of Hitachi LTD, Patent Abstract of Japan 05-052,721 ("Hitachi"). Claims 38, 39, 41, 42, 44 and 45 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hirose '971 and Hitachi and further in view of U.S. Patent No. 5,825,035 to Mizumura.

In accordance with the present response, claims 1 and 36-46 have been amended to further patentably distinguish from the prior art of record and to correct informalities. Claims 47-48 have been canceled, thereby rendering the Section 112, first paragraph, rejection of these claims moot. A new abstract which more clearly reflects the invention to which the amended claims are directed has been substituted for the previously submitted abstract.

Applicants request reconsideration of their application in light of the foregoing amendments and the following discussion.

The present invention relates to a method of preparing a sample chip and observing a wall surface of the sample chip.

Various conventional techniques for forming a sample chip and observing a surface of the sample chip are known. For example, as described in the specification (pgs. 1-3), the conventional techniques are complex and expensive to carry out. Additionally, the conventional techniques do not generate sufficient resolution for adequate observation of the surface of the sample chip. As a result, a comprehensive analysis of the sample chip (e.g., observation of the geometry of the surface of the sample chip) cannot be performed with the conventional techniques.

The present invention overcomes the drawbacks of the conventional art. With reference to the embodiment shown in Figs. 1A-1H, for example, a method of preparing a sample chip and observing a wall surface thereof according to the invention comprises a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a focused ion beam 2 to form a sample chip 1. Preferably, when the sample is made of different materials, a wall surface of the sample chip is gas-assist-etched during

irradiation with the focused ion beam 2 so that the wall surface is formed with stepped portions due to differences in etching rate of the materials forming the wall surface of the sample. Thereafter, in a second step, the sample chip is taken out from the sample. In a third step, the wall surface of the sample chip is observed with a scanning probe microscope. By this method, the geometry of the surface of the sample chip and its three-dimensional distribution thereof can be observed with an atomic level resolution.

Rejection of Claim 1
Under 35 U.S.C. §102(e)

Applicants respectfully traverse the rejection of claim 1 as being anticipated by Hirose '971.

Amended independent claim 1 is directed to a method of preparing a sample chip and observing a wall surface thereof. Amended claim 1 requires a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a focused ion beam to form a sample chip having a wall surface formed with stepped portions due to differences in etching rate of materials forming the wall surface, a second step of taking out the sample chip from the sample, and a third step of observing the wall surface of the sample chip with a scanning probe microscope. No corresponding combination of steps are disclosed or described by Hirose '971.

Hirose '971 discloses a method of observing the atomic condition or electron condition of a defective portion using a scanning probe microscope. However, Hirose '971 does not disclose or describe the formation of a sample chip having a wall surface formed with stepped portions due to differences in etching rate of materials forming the wall surface, as recited in amended independent claim 1.

Hirose '971 also fails to disclose or describe the provision of the wall surface of the sample chip with stepped portions as set forth above before the sample chip is taken out from the sample and subsequently observed with a scanning probe microscope, as recited in claim 1. By this sequence of steps, the stepped portions of the wall surface of the sample chip permits three-dimensional images of laminated structures of semiconductor IC's, for example, to be observed clearly.

Thus, Hirose '971 does not disclose or describe each element recited in amended independent claim 1 and, therefore, does not anticipate the claim under 35 U.S.C. §102(e). See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish unpatentability of the claimed invention

anticipation under § 102 can not be found"); Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim"). Furthermore, Hirose '971 does not suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Hirose '971's method to arrive at the claimed invention.

In view of the foregoing, applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §102(e) as being anticipated by Hirose '971 be withdrawn.

Rejection of Claims 36, 37, 40, 43, 46 Under 35 U.S.C. §103(a)

Applicants respectfully traverse the rejection of claims 36, 37, 40, 43 and 46 as being unpatentable over Hirose '971 in view of Hitachi.

Each of independent claims 36, 40 and 43 has been amended to incorporate subject matter recited in dependent claims 38, 41 and 44, respectively, in order to further distinguish from the combined teachings of Hirose '971 and Hitachi. More specifically, each of amended independent claims 36, 40 and 43 recites a third step of irradiating a wall surface of the sample chip with an argon ion beam to thereby etch the wall surface. No corresponding step is

disclosed or suggested by the combined teachings of Hirose '971 and Hitachi.

Moreover, with respect to the use of an argon ion beam recited in dependent claims 38, 41 and 44, now the subject matter of amended independent claims 36, 40 and 43, respectively, the Examiner cited Mizumura for its teaching of employing an argon ion beam as the focused energy beam because an argon ion beam can be irradiated onto a sample (e.g., a silicon wafer) without causing contamination of the sample with heavy metals. However, Mizumura does not disclose or suggest the irradiation of a wall surface (i.e., etching the wall surface) of a sample chip with an argon ion beam (third step) after the sample from which the sample chip is formed has been processed (i.e., has been irradiated) with a focused energy beam (first step), as recited in each of independent claims 36, 40 and 43.

Claims 37 and 46 depend on and contain all of the limitations of amended independent claims 36 and 43, respectively, and, therefore, distinguish from the references at least in the same manner as claims 36 and 43.

Moreover, there is a separate ground for patentability of amended dependent claim 37 which includes the additional limitation that the argon ion beam is irradiated from a tangent direction of the wall surface. No corresponding step is disclosed or suggested by the prior art of record.

In view of the foregoing, applicants respectfully request that the rejection of claims 36, 37, 40, 43 and 46 as being unpatentable over Hirose '971 in view of Hitachi be withdrawn.

Rejection of Claims 38, 39, 41, 42, 44 and 45 Under 35 U.S.C. §103(a)

Applicants respectfully traverse the prior art rejection of claims 38, 39, 41, 42, 44 and 45 based on the teachings of Hirose '971, Hitachi and Mizumura.

Hirose '971 in view of Hitachi does not disclose or suggest the combination of steps recited in independent claims 36, 40 and 43 as set forth above for the rejection of claims 36, 37, 40, 43 and 46 under 35 U.S.C. §103(a). Claims 38-39, 41-42 and 44-45 depend on and contain all of the limitations of amended independent claims 36, 40 and 43, respectively, and, therefore, distinguish from the references at least in the same manner as claims 36, 40 and 43.

Mizumura does not cure the deficiencies of Hirose '971 as modified by Hitachi. In this regard, Mizumura does not teach the combination of the first and third steps recited in amended independent claims 36, 40 and 43, from which claims 38-39, 41-42 and 44-45 respectively depend as set for above amended claims 36, 40 and 43. Accordingly, one of ordinary skill in the art would not have been led to modify the references to attain the claimed subject matter.

Moreover, there are separate grounds for patentability of dependent claims 39, 42 and 45 which are directed to the formation of stepped portions in the wall surface of the sample chip due to differences in etching rate in materials forming the wall surface of the sample chip. No corresponding step is disclosed or suggested by the prior art of record as set forth above for amended independent claim 1.

In view of the foregoing, applicants respectfully request that the rejection of claims 38, 39, 41, 42, 44 and 45 based on the teachings of Hirose '971, Hitachi and Mizumura be withdrawn.

In view of the foregoing, applicants respectfully submit that pending claims 1 and 36-46 patentably distinguish over the prior art. Accordingly, favorable reconsideration and withdrawal of the prior art rejections together with passage of the application to issue are respectfully requested.

Respectfully submitted,

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